PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-AAS/13/7894
Dated 27 May 2013

L272 family Wafer Diameter change

Table 1. Change Implementation Schedule

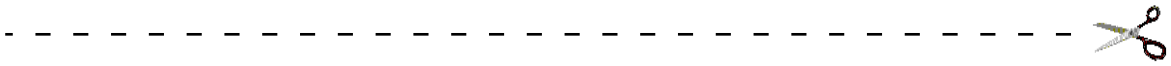
Forecasted implementation date for change	20-May-2013
Forecasted availability date of samples for customer	30-May-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	20-May-2013
Estimated date of changed product first shipment	26-Aug-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	L272M; L2720W; L2722; L2726
Type of change	Waferfab process change
Reason for change	To increase production capacity
Description of the change	the wafer diameter for the products belonging to the L272 family , diffused on bipolar LAMT process, will be changed from 5" to 6" . Note: with the agreement of the customer, parts from 6" wafers can be delivered even in advance in respect of the scheduled date.
Change Product Identification	Traceability code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN AMS-AAS/13/7894**
Please sign and return to STMicroelectronics Sales Office	**Dated 27 May 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Ferri, Simone	Marketing Manager
Onetti, Andrea Mario	Product Manager
Speroni, Ernesto Fabrizio	Q.A. Manager

L272 family Wafer Diameter change

WHAT

As part of the running program to convert to 6” wafers the silicon lines diffused on the bipolar processes in the Ang Mo Kio plant, the wafer diameter for the products belonging to the L272 family (see attached product list) , diffused on bipolar LAMT process, will be changed from 5” to 6”

WHY

To rationalize the production capacity.

HOW

The bipolar diffusion process family is qualified and running in volumes on 6” wafers.
The qualification has been done through test vehicles belonging to the same bipolar process family (namely LM317) and to the same silicon lines (namely L272D and L2722). The related reports are attached.
The alignment of electrical parameters of the impacted devices will be monitored as well.

Note: with the agreement of the customer, parts from 6” wafers can be delivered even in advance in respect of the scheduled date.

Reliability Report

L272 and L372: wafer diameter change from 5” to 6”

General Information	
Product Lines	*L272 and L372*
Product Description	*Dual power operational amplifier*
Finished Good Codes	*L272D ; L2722*
Product division	*AMS Analog and Audio Systems*
Package	*PDIP8 ; SO16*
Silicon process technology	*BIP>6um - MT*
Raw Line Code :	*A3Q7*L272AAE ; C58W*L372FAE*

Locations	
Wafer fab location	*AMJ9*
Assembly fab location	*Amkor ; Shenzen*
Reliability assessment	*Passed*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	16/05/2013	7	Fabio Fiabane	

Issued by **Fabio Fiabane**

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on *L272* and *L372* in order to qualify the MT process in AMJ9 – 6" line (wafer diameter change).
This process is already qualified in AMJ9 – 5" line.

Preliminary conditions:
- No other change than wafer diameter.
- Process alignment verification in physical and electrical (T84) parameters.
- Electrical device parameters verification (ED).

1.2 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.

Package oriented tests have not put in evidence any criticality regarding the FE/BE compatibility.

Furthermore, the qualification of the similar process LAAT in AMJ9 with the test vehicle L317 (reliability report REL - 6043- 189.11W) must be considered to reinforce the reliability assessment.

On the ground of the overall positive results we can conclude that *L272 and L372* devices , diffused in AMJ9, can be released to production, from a reliability point of view.

2 DEVICE CHARACTERISTICS

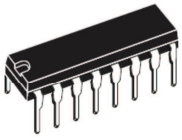
2.1 Device description

2.1.1 Generalities L2722

L2720/2/4

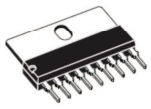
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1 A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE



POWERDIP
(8 + 8)

MINIDIP
(Plastic)



SIP9

ORDERING NUMBERS : L2720 (Powerdip)
L2722 (Minidip)
L2724 (SIP9)

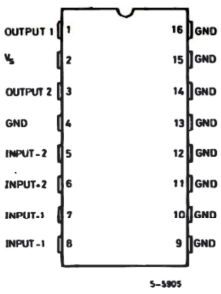
DESCRIPTION

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

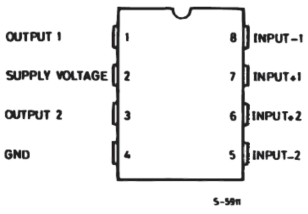
They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

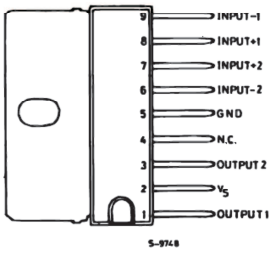
PIN CONNECTIONS (top views)



L2720



L2722



L2724

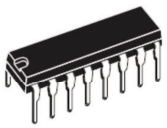
July 2003 1/10

2.1.2 Generalities L272D

L272

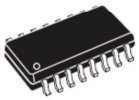
DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1 A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN



Powerdip
(8 + 8)

Minidip



SO16 (Narrow)

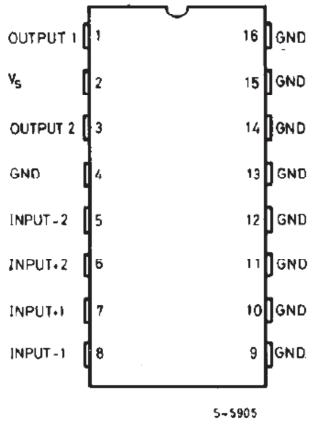
ORDERING NUMBERS : L272 (Powerdip)
L272M (Minidip)
L272D (SO16 Narrow)

DESCRIPTION

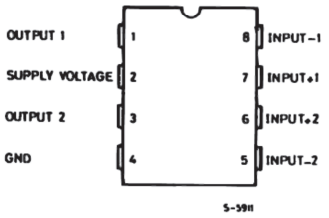
The L272 is a monolithic integrated circuits in Powerdip, Minidip and SO packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compacts disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

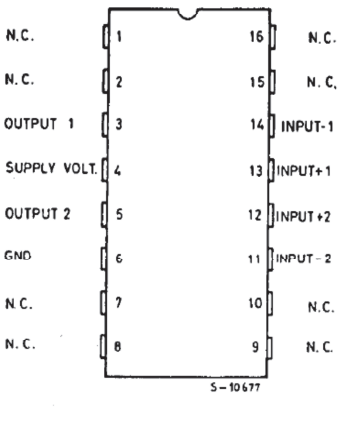
PIN CONNECTIONS (top view)



L272



L272M



L272D

2.2 Traceability

Wafer fab information		
Device	*L272*	*L372*
Wafer fab manufacturing location	*AMJ9*	
Wafer diameter	*6*	
Silicon process technology	*BIP (>6um) - MT/-K (10/1m)*	
Die finishing back side	*CHROMIUM/NICKEL/GOLD*	
Die size [µm x µm]	*1910 x 2450*	*2420 x 2140*
Metal levels	*1*	

Assembly Information		
Device	*L272*	*L372*
Assembly fab location	*ST Shenzen*	*Amkor*
Package description	*SO 16*	*PDIP 8*

3 TESTS DESCRIPTION & DETAILED RESULTS

3.1 Die and Package tests description

TEST NAME	DESCRIPTION	PURPOSE
HTB: High Temperature Bias	The device is stressed in static configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias.	To simulate the worst-case application stress conditions. The test is oriented to investigate typical IC failure modes like oxide faults and metal degradation and to check overall IC the parametric stability.
PC (JL3): Preconditioning (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.	To investigate in general the effect of customer manufacturing soldering enhanced by package water absorption. As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.
TC: Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding wire-bonds failure.

3.2 LOT Information

Qualification lot number	RL code	Diffusion Lot Number	Package
1	*A3Q7*L272AAE*	*W226N4E*	*SO16*
2	*C58W*L372FAE*	*W226N4H*	*PDIP8*

3.3 Detailed results

N	TEST NAME	CONDITION/METHOD	STEPS	FAILS/SS	
				LOT 1	LOT 2
1	**HTB**	Reference specification = JESD22-A108 125 ºC Tj as minimum at Vcc Max	500 H	0 / 77	0 / 77
			1000 H	0 / 77	0 / 77
2	**Preconditioning ML3**	Reference specification = JEDEC J-STD-020	Final	0/40	-
3	**TC**	Ta Cycling: -50°C/+150°C Reference specification = JESD22a104	500 Cy	0 / 77	0 / 77
			1000 Cy	0 / 77	0 / 77

Internal Reliability Evaluation Report

Qualify AMK5 versus **AMJ9 6"**

[LAAT100 Technology]

T.V: L317AAW – LM317 D2PAK

General Information	
Product Line	L317AAW
Product Description	Linear Voltage Regulator
P/N	LM317D2T-TR$1Z
Product Group	APM
Product division	IPC
Package	D2PAK CENTRAL LEAD CUT
Silicon Process technology	LAAT100
Production mask set rev.	NL317A6

Locations	
Wafer fab	*AMJ9 6"*
Assembly plant	*ST SHENZHEN -CHINA*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	13-Jul-2011	9	Alfio Rao Giuseppe Giacopello	G. Presti	Final

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

LAAT100 Bipolar Technology diffused in AMJ9 6" (Transferring project).

TV: L317AAW - LM317D2T-TR$1Z assembled in D2pak.

Shared qualification

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime

.

4 DEVICE CHARACTERISTICS

4.1 Device description

Features

- Output voltage range: 1.2 to 37 V
- Output current in excess of 1.5 A
- 0.1 % line and load regulation
- Floating operation for high voltages
- Complete series of protections: current limiting, thermal shutdown and SOA control

Description

The LM117, LM217, LM317 are monolithic integrated circuits in TO-220, TO-220FP, TO-3 and D²PAK packages intended for use as positive adjustable voltage regulators. They are designed to supply more than 1.5 A of load current with an output voltage adjustable over a 1.2 to 37 V range. The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

D²PAK

4.2 Construction note

.

	P/N: LM317D2T-TR$1Z
Wafer/Die fab. information	
Wafer fab manufacturing location	AMJ9 6"
Technology	LAAT100
Process family	C4-BIP (>6um)
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	2.410X1.920mm2
Bond pad metallization layers	AlSi
Passivation type	SiN (nitride)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK6
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	D2PAK CENTRAL LEAD CUT
Molding compound	RESIN SUMITOMO EME-G620A D18mm W10.2g
Frame material	TO263 Dt 40u Ver7 OptF/G SelNiNiP
Die attach process	Pb/Ag/Sn 95.5/2.5/2 D.76mm SSD
Die pad size	150umx150um
Wire bonding process	N.A.
Wires bonding materials/diameters	Cu 2,0 MILS
Final testing information	
Testing location	ST SHENZHEN -CHINA
Tester	QT200
Test program	LX17FC.CTS

TESTS RESULTS SUMMARY

4.3 Test plan and results

P/N: LM317D2T-TR$1Z

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line	Comments
1	W047K36B	GK107PJ01	HZDJ*L317AAW	D2PAK CENTRAL LEAD CUT	L317AAW	

Results summary

P/N: LM317D2T-TR$1Z

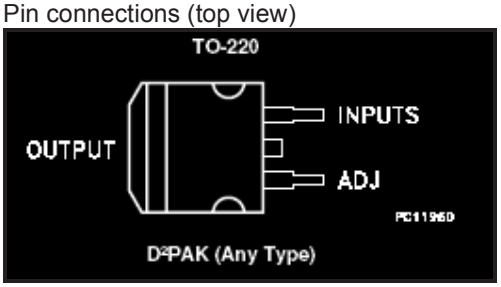
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTOL	N	JESD22 A-108	Tj = 125℃, BIAS=35 V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	Ta = 150℃	45	168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times	400	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77	168 H	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃ Air to air	77	100 cy	0/77	
					300 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS=24V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	

5 ANNEXES

5.1 Device details

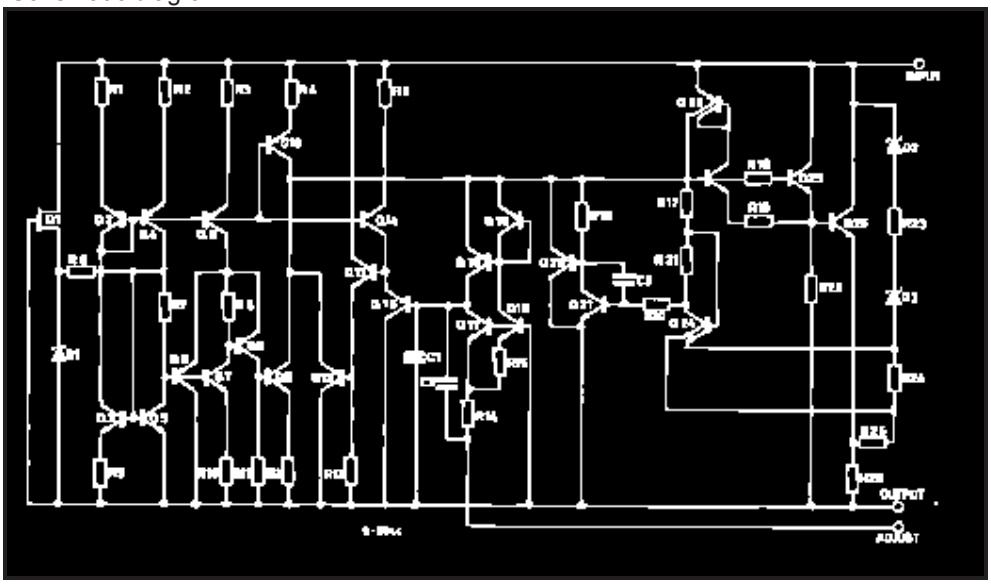
5.1.1 Pin connection

Pin connections (top view)



5.1.2 Block diagram

Schematic diagram

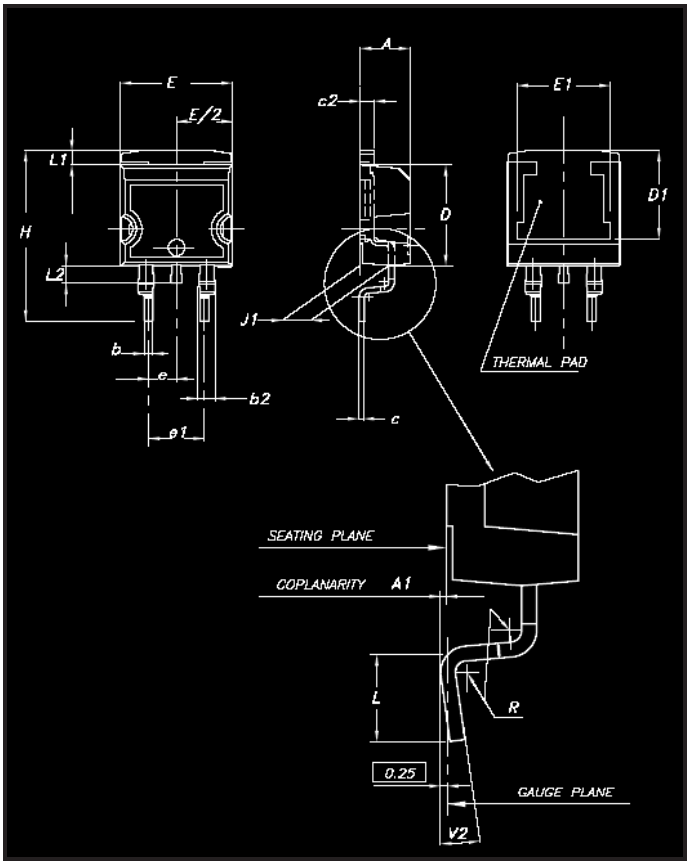


5.1.3 Bonding diagram

8314205

5.1.4 Package outline/Mechanical data

Drawing dimension D²PAK (type STD-ST)



D²PAK mechanical data

Dim.	Type STD-ST		
	mm.		
	MIN.	TYP.	MAX.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

5.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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